

WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor integrated circuit, said method comprising:

a) forming a device isolation layer at a semiconductor substrate to define first and second active regions;

b) forming a plurality of first gate patterns that extend across the first active region, regions between the first gate patterns including a first space having a first width and a second space having a second width greater than the first width;

c) selectively removing the device isolation layer exposed by the first space;

d) forming a line-shaped first impurity region and an island-shaped second impurity region at the surface of the semiconductor substrate exposed by the first space and at the first active region exposed by the second space, respectively;

e) forming a second gate pattern that extends across the second active region;

f) forming low concentration source/drain regions at the second active region located on both sides of the second gate pattern to provide LDD-type source/drain regions;

g) forming spacers on sidewalls of the second space and on sidewalls of the second gate pattern as well as a spacer layer pattern filling the first space;

h) forming high concentration source/drain regions adjacent the low concentration source/drain regions at the second active region;

i) removing said spacers to expose the sidewalls of the second space and the second gate pattern and to remain a recessed spacer layer pattern in the first space; and

j) forming a conformal etching stop layer on the semiconductor substrate having the recessed spacer layer pattern.

2. The method of claim 1, wherein the first active region is defined in a first region of the semiconductor substrate and the second active region is defined in a second region of the semiconductor substrate.

3. The method of claim 1, wherein the device isolation layer is formed using a trench isolation technique.

4. The method of claim 1, wherein selectively removing the device isolation layer exposed by the first space comprises:

a) forming a photoresist pattern that exposes the first space; and

b) etching the device isolation layer using the photoresist pattern as an etch mask until the semiconductor substrate contacting the device isolation layer in the first space is exposed.

5 5. The method of claim 4, wherein forming the first and second impurity regions comprises:

a) implanting first impurity ions into the semiconductor substrate exposed by the first space using the photoresist pattern as an ion implantation mask;

b) removing the photoresist pattern; and

10 c) implanting second impurity ions into the semiconductor substrate exposed by the first space and the second space using the first gate patterns and the device isolation layer as an ion implantation mask.

6. The method of claim 1, wherein forming the spacers and the spacer layer pattern comprises:

15 a) forming a spacer layer on the semiconductor substrate having the low concentration source/drain regions, the spacer layer being formed to a thickness which is greater than half of the first width and less than half of the second width; and

b) anisotropically etching the spacer layer to expose the second impurity region and the low concentration source/drain regions and to concurrently remain anisotropically etched
20 spacer layer that fills the first space.

7. The method of claim 6, wherein the spacer layer comprises silicon nitride.

25 8. The method of claim 7, further comprising forming a conformal stress buffer oxide layer on the semiconductor substrate having the low concentration source/drain regions before forming the spacer layer.

9. The method of claim 1, further comprising forming an interlayer insulating layer on the semiconductor substrate having the etching stop layer.

30 10. The method of claim 9, wherein the etching stop layer is formed of an insulating layer that has an etching selectivity with respect to the interlayer insulating layer.

11. The method of claim 9, further comprising:

- a) patterning the interlayer insulating layer and the etching stop layer to form a first contact hole exposing the LDD-type source/drain regions and the second gate pattern;
- b) patterning the interlayer insulating layer and the etching stop layer to form a second contact hole exposing the second impurity region;
- 5 c) selectively applying a plug ion implantation process to the second impurity region exposed by the second contact hole;
- d) forming contact plugs that fill the first and second contact holes; and
- e) forming metal interconnection lines on the interlayer insulating layer, the metal interconnection lines being formed to cover the contact plugs.

- 10 12. A method of manufacturing a flash memory device, the method comprising:
- a) providing a semiconductor substrate having a cell array region and a peripheral circuit region;
 - b) forming a device isolation layer at a portion of the semiconductor substrate to
15 define a cell active region in the cell array region and a peripheral circuit active region in the peripheral circuit region;
 - c) forming a stacked gate layer on the cell array region and a peripheral circuit gate layer on the peripheral circuit region;
 - d) patterning the stacked gate layer to form a plurality of stacked gate patterns that
20 extend across the cell active region, regions between the stacked gate patterns including first spaces having a first width and second spaces having a second width greater than the first width;
 - e) selectively removing a portion of the device isolation layer exposed by the first spaces;
 - 25 f) forming line-shaped common source regions and island-shaped drain regions at the surface of the semiconductor substrate exposed by the first spaces and at the surface of the cell active region exposed by the second spaces, respectively;
 - g) patterning the peripheral circuit gate layer to form a peripheral circuit gate electrode extending across the peripheral circuit active region;
 - 30 h) implanting impurity ions into the peripheral circuit active region, using the peripheral circuit gate electrode, as an ion implantation mask to form low concentration source/drain regions at the peripheral circuit active region;
 - i) forming spacer layer patterns filling the first spaces as well as spacers covering sidewalls of the second spaces and also sidewalls of the peripheral circuit gate electrode;

j) forming high concentration source/drain regions at the peripheral circuit active region, using the peripheral circuit gate electrode and the spacer on the sidewall of the peripheral circuit gate electrode as ion implantation masks, thereby providing LDD-type source/drain regions;

5 k) removing the spacers to expose the sidewalls of the second spaces and the sidewall of the peripheral circuit gate electrode and to concurrently remain recessed spacer layer patterns in the first spaces; and

l) forming a conformal etching stop layer on the semiconductor substrate having the recessed spacer layer patterns.

10 13. The method of claim 12, wherein forming the device isolation layer comprises:

a) forming first and second trench mask patterns on the semiconductor substrate in the cell array region and on the semiconductor substrate in the peripheral circuit region
15 respectively;

b) etching the semiconductor substrate using the first and second trench mask patterns as etching masks to form a cell trench region in the cell array region and a peripheral circuit trench region in the peripheral circuit region; and

c) forming a cell device isolation layer in the cell trench region and a peripheral
20 circuit device isolation layer in the peripheral circuit trench region.

14. The method of claim 13, wherein forming the first and second trench mask patterns comprises:

a) sequentially forming a gate insulating layer and a lower gate conductive layer on
25 the semiconductor substrate;

b) patterning the lower gate conductive layer and the gate insulating layer to expose the semiconductor substrate in the cell array region;

c) sequentially forming a tunnel insulating layer and a lower floating gate layer on the exposed semiconductor substrate;

30 d) forming a trench mask layer on the semiconductor substrate having the lower floating gate layer and the lower gate conductive layer, the trench mask layer being formed by sequentially stacking a polishing stop layer and a hard mask layer; and

e) patterning the trench mask layer.

15. The method of claim 13, wherein forming the cell trench region and the peripheral circuit trench region comprises:

a) forming a photoresist pattern covering the cell array region on the semiconductor substrate having the first and the second trench mask patterns;

5 b) etching the semiconductor substrate, using the photoresist pattern and the second trench mask pattern as etching masks, to form a preliminary peripheral circuit trench region in the peripheral circuit region;

c) removing the photoresist pattern; and

10 d) etching the semiconductor substrate using the first and second trench mask patterns as etching masks to form a trench region having a first depth and another trench region having a second depth greater than the first depth in the cell array region and the peripheral circuit region, respectively.

16. The method of claim 14, wherein forming the stacked gate layer and the peripheral circuit gate layer comprises:

a) removing the patterned trench mask layer to expose the lower floating gate layer and the lower gate conductive layer;

b) forming an upper floating gate pattern covering the exposed lower floating gate layer and a first upper gate conductive layer covering the peripheral circuit region; and

20 c) sequentially forming an inter-gate dielectric layer and a first control gate conductive layer on the cell array region having the upper floating gate pattern.

17. The method of claim 16 further comprising forming a metal silicide layer on the first control gate conductive layer and the first upper gate conductive layer.

18. The method of claim 12, wherein selective removing the device isolation layer exposed by the first spaces comprises:

a) forming a photoresist pattern exposing the first spaces on the semiconductor substrate having the stacked gate patterns; and

30 b) etching the device isolation layer, using the photoresist pattern as an etching mask, to expose the semiconductor substrate that contacts the device isolation layer in the first spaces.

19. The method of claim 18, wherein forming the common source regions and the drain regions comprises:

a) implanting first impurity ions into the semiconductor substrate exposed by the first spaces, using the photoresist pattern as an ion implantation mask;

5 b) removing the photoresist pattern; and

c) implanting second impurity ions into the semiconductor substrate in the cell array region, using the stacked gate patterns and the device isolation layer as ion implantation masks.

10 20. The method of claim 12, wherein forming the spacers and the spacer layer patterns comprises:

a) forming a spacer layer on the semiconductor substrate having the low concentration source/drain regions to a thickness greater than half of the first width and less than half of the second width; and

15 b) anisotropically etching the spacer layer to expose the drain regions and the low concentration source/drain regions and to concurrently remain the anisotropically etched spacer layer that fills the first spaces.

21. The method of claim 20, wherein the spacer layer is formed of silicon nitride.

20 22. The method of claim 21, further comprising forming a conformal stress buffer oxide layer on the semiconductor substrate having the low concentration source/drain regions before forming the spacer layer.

25 23. The method of claim 12, further comprising forming an interlayer insulating layer on the etching stop layer.

24. The method of claim 23, wherein the etching stop layer is formed of an insulating layer having an etching selectivity with respect to the interlayer insulating layer.

30 25. The method of claim 23, further comprising:

a) patterning the interlayer insulating layer and the etching stop layer to form first contact holes exposing the LDD-type source/drain regions and the peripheral circuit gate electrode;

b) patterning the interlayer insulating layer and the etching stop layer to form second contact holes exposing the drain regions in the cell array region;

c) selectively applying a plug ion implantation process to the drain regions exposed by the second contact holes;

5 d) forming contact plugs that fill the first and second contact holes; and

e) forming metal interconnection lines on the interlayer insulating layer, the metal interconnection lines being formed to cover the contact plugs.

26. A semiconductor integrated circuit device comprising:

10 a device isolation layer formed at a semiconductor substrate to define first and second active regions;

a plurality of first gate patterns extending across the first active region, regions between the gate patterns including a first space having a first width and a second space having a second width greater than the first width;

15 a line-shaped first impurity region formed at the surface of the semiconductor substrate under the first space;

an island-shaped second impurity region formed at the surface of the first active region under the second space;

a second gate pattern extending across the second active region;

20 a recessed spacer layer pattern filling the first space overlying the first impurity region;

LDD-type source/drain regions formed at the second active region on both sides of the second gate pattern; and

25 a conformal etching stop layer overlying the semiconductor substrate having the recessed spacer layer pattern and the LDD-type source/drain regions.

27. The semiconductor integrated circuit device of claim 26, further comprising a stress buffer oxide layer interposed between the recessed spacer layer pattern and the first impurity region as well as between the recessed spacer layer pattern and the first gate patterns, wherein the stress buffer oxide layer is extended to cover the surfaces of the first gate patterns, the surface of the second impurity region, the surface of the device isolation layer, the surface of the second gate pattern and the surfaces of the LDD-type source/drain regions.

30

28. The semiconductor integrated circuit device of claim 26, further comprising an interlayer insulating layer formed on the etching stop layer.

29. The semiconductor integrated circuit device of claim 28, wherein the etching stop layer is an insulating layer having an etching selectivity with respect to the interlayer insulating layer.

30. The semiconductor integrated circuit device of claim 28, further comprising contact plugs that penetrate the interlayer insulating layer and the etching stop layer to contact the second impurity region, the second gate pattern and the LDD-type source/drain regions.

31. A flash memory device comprising:
a semiconductor substrate having a cell array region and a peripheral circuit region;
a device isolation layer formed at the semiconductor substrate to define a cell active region in the cell array region and a peripheral circuit active region in the peripheral circuit region;

a plurality of stacked gate patterns extending across the cell active region, regions between the stacked gate patterns including first spaces having a first width and second spaces having a second width greater than the first width;

line-shaped common source regions formed at the surface of the semiconductor substrate under the first spaces;

island-shaped drain regions formed at the surface of the cell active region under the second spaces;

a peripheral circuit gate electrode extending across the peripheral circuit active region;

recessed spacer layer patterns filling the first spaces and overlying the common source regions;

LDD-type source/drain regions formed at the peripheral circuit active region located on both sides of the peripheral circuit gate electrode; and

a conformal etching stop layer overlying the semiconductor substrate having the recessed spacer layer patterns and the LDD-type source/drain regions.

32. The flash memory device of claim 31, wherein the device isolation layer includes a cell device isolation layer formed in the cell array region and a peripheral circuit device isolation layer formed in the peripheral circuit region, the peripheral circuit device isolation layer being deeper than the cell device isolation layer.

5

33. The flash memory device of claim 31, further comprising a stress buffer oxide layer located between the recessed spacer layer pattern and the common source region as well as between the recessed spacer layer pattern and the stacked gate pattern, wherein the stress buffer oxide layer covers the surfaces of the stacked gate patterns, the surfaces of the drain regions, the surface of the device isolation layer, the surface of the peripheral circuit gate electrode and the surfaces of the LDD-type source/drain regions.

10

34. The flash memory device of claim 31, further comprising an interlayer insulating layer formed on the etching stop layer.

15

35. The flash memory device of claim 34, wherein the etching stop layer is an insulating layer having an etching selectivity with respect to the interlayer insulating layer.

36. The flash memory device of claim 34, further comprising contact plugs that penetrate the interlayer insulating layer and the etching stop layer to contact the drain regions, the peripheral circuit gate electrode and the LDD-type source/drain regions.

20

37. A semiconductor integrated circuit device formed by a process comprising:

a) forming a device isolation layer at a semiconductor substrate to define first and second active regions;

25

b) forming a plurality of first gate patterns extending across the first active region, the plurality of the first gate patterns defining a first space and a second space therebetween, the second space being wider than the first space, the first space exposing a portion of the device isolation layer;

c) selectively removing the portion of the device isolation layer exposed by the first space;

30

d) forming a first impurity region and a second impurity region at the surface of the semiconductor substrate exposed by the first space and at the first active region exposed by the second space, respectively;

e) forming a second gate pattern that extends across the second active region;
f) forming low concentration source/drain regions at the second active region located on both sides of the second gate pattern; and
g) forming spacers on sidewalls of the second space and on sidewalls of the second gate pattern as well as a spacer layer pattern filling the first space;
h) forming high concentration source/drain regions adjacent the low concentration source/drain regions at the second active region to provide LDD-type source/drain regions; and
i) removing said spacers to expose the sidewalls of the second space and the second gate pattern and to concurrently remain a recessed spacer layer pattern in the first space; and
j) forming a conformal etching stop layer on the semiconductor substrate having the recessed spacer layer pattern.

38. The device of claim 37, wherein the first impurity region is line-shaped.

39. The device of claim 37, wherein the second impurity region is island-shaped.